REMARKS

The Examiner noted that it is the applicant's duty to particularly point out any highly relevance material amongst the references cited in the IDS. Applicant considers such a request to be made under 37 C.F.R. 1.105. In response, applicant asserts that the information requested to be submitted is unknown and/or is not readily available.

The Examiner has objected to the Specification due to informalities. Specifically, the Examiner argued that "DBin and DBout are not exclusively defined on page 9, lines 23-28" and that "[b]oth are defined as the width of Data Bus 310." Applicant respectfully asserts that such objection is avoided in view of the clarification made to the specification.

The Examiner has objected to Claims 1-13 due to informalities. Applicant respectfully asserts that such objections are avoided in view of the clarifications made to the claims.

The Examiner has rejected Claims 1-4, 6-7, and 11-13 under 35 U.S.C. 102(e) as being anticipated by Chadalapaka (U.S. Patent No. 6,845,403). Applicant respectfully disagrees with such rejection.

With respect to independent Claim 1, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed "outputting said data blocks from said buffer while counting the number of data blocks that have been stored in said registers" (as amended).

> "The initiator and target are assumed to have three counters that define the allocation mechanism--CmdRN--the current command reference number advanced by 1 on each command shipped--ExpCmdRN--the next expected command by the target--acknowledges all commands up to it--MaxCmdRN--the maximum number to be shipped--MaxCmdRN--ExpCmdRN defines the queuing capacity of the receiving iSCSI layer." (Chadalapaka, Col. 6, lines 23-30 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely teaches that "[t]he initiator and target are assumed to have three counters that define the allocation mechanism" (emphasis added). Further, Chadalapaka teaches that three counters are: CmdRN, which counts the commands shipped, ExpCmdRN, which is the next expected command by the target, and MAXCmdRN, which is the maximum number of commands to be shipped. However, the mere disclosure by Chadalapaka that the initiator and target have three counters (CmdRN, ExpCmdRN, and MaxCmdRN) which define the allocation mechanism fails to even suggest "outputting said data blocks from said buffer **while** counting the number of data blocks that have been stored in said registers" (emphasis added), as claimed by applicant. Clearly, Chadalapaka's command counters fail to even suggest "counting the number of data blocks that have been stored in said registers" (emphasis added), in the manner as claimed by applicant

Further, with respect to independent Claim 1, the Examiner has relied on the following excerpts from the Chadalapaka reference to make a prior art showing of applicant's claimed "inserting interval markers between said data blocks at predetermined intervals within said data stream prior to outputting said data blocks, said predetermined intervals determined in accordance with the number of data blocks counted and a desired marker interval" (as amended).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

> 'At fixed intervals in the TCP byte stream, a "Marker" is inserted. This Marker indicates the offset to the next iSCSI message header. The Marker is eight bytes in length, and contains two 32-bit offset fields that indicate how many bytes to skip in the TCP stream to find the next iSCSI message header.' (Chadalapaka, Col. 10, lines 46-51 - emphasis added)

Applicant respectfully asserts that the excerpts from Chadalapaka relied upon by the Examiner merely disclose that '[a]t fixed intervals in the TCP byte stream, a "Marker"

is inserted' (emphasis added). In addition, Chadalapaka teaches that "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream" (emphasis added). However, the mere disclosure in Chadalapaka that a marker is placed at fixed intervals to reduce the amount of temporary buffering and copying simply fails to even suggest that "said predetermined intervals [are] **determined** in accordance with the number of data blocks counted and a desired marker interval" (emphasis added), as claimed by applicant. Clearly, the mere disclosure of fixed intervals fails to even suggest "predetermined intervals" which are "determined in accordance with the number of data blocks counted" (emphasis added), as claimed by applicant.

With respect to independent Claim 4, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed "inserting interval markers between data blocks stored in said registers as specified by said parameters, and indicated by said block count value and said marker offset value" (as amended).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely discloses that in order "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream" (emphasis added). However, the mere disclosure that the markers are placed at fixed intervals in the TCP stream fails to even suggest "inserting interval markers between data blocks stored in said registers as specified by said parameters, and indicated by said block count value and said marker offset value" (emphasis added), as claimed by applicant. Clearly, the fixed interval markers as disclosed by Chadalapaka fail to teach that the "interval markers [are inserted] between data blocks ... indicated by

said block count value and said marker offset value" (emphasis added), as claimed by applicant.

With respect to independent Claim 11, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed "inserting said interval markers between data blocks stored in said registers as indicated by said block count value and said marker offset value" (as amended).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely discloses that in order "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream" (emphasis added). However, the mere disclosure that the markers are placed at fixed intervals in the TCP stream fails to even suggest "inserting said interval markers between data blocks stored in said registers as indicated by said block count value and said marker offset value" (emphasis added), as claimed by applicant. Clearly, teaching that the markers are placed at fixed intervals fails to even suggest that the "interval markers [are inserted] ... as indicated by said block count value and said marker offset value" (emphasis added), as claimed by applicant.

With respect to independent Claim 12, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed "a marker generator for inserting interval markers at predetermined intervals between data blocks stored in said buffer, said predetermined intervals determined in accordance with a number of data blocks counted and a desired marker interval" (as amended – emphasis added).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed

> intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely teaches that in order "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream" (emphasis added). However, the mere teaching that the markers are placed at fixed intervals in the TCP stream fails to even suggest "a marker generator for inserting interval markers at predetermined intervals between data blocks stored in said buffer, said predetermined intervals determined in accordance with a number of data blocks counted and a desired marker interval" (emphasis added), as claimed by applicant. Clearly, teaching that the markers are placed at fixed intervals fails to even suggest that the "predetermined intervals [are] determined in accordance with a number of data blocks counted and a desired marker interval" (emphasis added), as claimed by applicant.

With respect to independent Claim 13, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed "a marker insertion module for inserting interval markers at predetermined intervals between said data blocks stored in said buffer as indicated by said second counter" (as amended).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely discloses that in order "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream" (emphasis added). However, the mere disclosure that the markers are placed at fixed intervals in the TCP stream fails to even suggest "a marker insertion module for inserting interval markers at predetermined intervals between said data blocks

stored in said buffer as indicated by said second counter" (emphasis added), as claimed by applicant. Clearly, placing markers at fixed intervals fails to disclose "inserting interval markers at predetermined intervals ... as indicated by said second counter" (emphasis added), as claimed by applicant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the above reference, as noted above. Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to Claim 2, the Examiner has relied on the following excerpt from the Chadalapaka reference to make a prior art showing of applicant's claimed technique "wherein the number of said predetermined registers in said buffer is optimized to include a sufficient number of registers to receive and output data blocks, and registers for interval marker insertion" (as amended).

> "To reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP stream to enable accelerated iSCSI/TCP implementations to find and delineate iSCSI messages in the presence of IP packet reordering." (Chadalapaka, Col. 10, lines 34-39 - emphasis added)

Applicant respectfully asserts that the excerpt from Chadalapaka relied upon by the Examiner merely discloses that "[t]o reduce the amount of temporary buffering and copying, synchronization information (markers) is placed at fixed intervals in the TCP

stream" (emphasis added). However, the mere disclosure in Chadalapaka that a marker is placed at fixed intervals to reduce the amount of temporary buffering and copying simply fails to even suggest a technique "wherein the number of said predetermined registers in said buffer is optimized to include a sufficient number of registers to receive and output data blocks, and registers for interval marker insertion" (emphasis added), as claimed by applicant. Clearly, the except from Chadalapaka fails to suggest that the "predetermined registers in said buffer is optimized to include a sufficient number of registers to receive and output data blocks, and registers for interval marker insertion" (emphasis added), as claimed by applicant.

Again, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

To this end, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP340/P001325).

Respectfully submitted,
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